REMARKS

I. Introduction

With the addition of claims 29 to 33, claims 1 to 33 are now pending.

Applicants thank the Examiner for considering the previously filed Information Disclosure Statement, PTO-1449 paper and cited references.

II. Oath/Declaration

With respect to paragraph three (3) of the Office Action, the statement is not really understood. The Declaration(s) filed on July 13, 2001 include a post office address for each of the inventors, and the declaration(s) designate the Kenyon & Kenyon address to which all correspondence is to be sent. As to the original application papers, the address provided was the same Kenyon & Kenyon address. It is believed that Rule 33(a) is therefore satisfied, unless it can be explained what is further required.

III. Drawings

With respect to paragraph four (4) of the Office Action, the drawings of the Figures were objected to under 37 C.F.R. § 1.84(p)(5) for not including reference signs "289" and "300", which were mentioned in the description. The Specification has been amended on page 7, line 15, to remove the reference to "289" and replace it with a reference to "280", which is included in Figure 2. Figure 3 has been amended to include reference numeral "300".

With respect to paragraph five (5) of the Office Action, the drawings of the Figures were objected to under 37 C.F.R. § 1.84(p)(5) for including reference signs 285, 410, 420, and 430, which were not mentioned in the description. The Specification has been amended on page 7, line 14, to include a reference to "285". The Specification has also been amended on page 13, lines 16 and 17, to include reference to "410", "420", and "430".

With respect to paragraph six (6) of the Office Action, the drawings of the Figures were objected under 37 C.F.R. § 1.84(p)(4) for using reference "280" in the Specification and reference "285" in Figure 2 to designate the wide multiplexer of Figure 2. The Specification has been amended on page 7, line 14, to replace the reference to "280".

With respect to paragraphs seven (7), the drawings of the Figures were objected to for using handwritten figure titles and reference numerals, and for the use of shading. Although the objections may not be agreed with, to facilitate matters, it is believed that the proposed drawing corrections and/or amendments accompanying should obviate all of the objections, since they are believed to reflect the suggestions of the Examiner.

In sum, it is believed that all objections with respect to the Figures have been addressed. It is therefore respectfully requested that the objections to the drawings be withdrawn, and that the drawing amendments be entered using the Replacement sheets for Figures 1 to 6.

IV. Title

The title has been revised along the lines suggested. Approval and entry are respectfully requested.

V. Rejection of claims 1 to 28 under 35 U.S.C. § 102(b)

Claims 1 to 28 stand rejected under 35 U.S.C. § 102(b) as anticipated by Vajapeyam et al., "Improving Superscalar Instruction Dispatch and Issue by Exploiting Dynamic Code Sequences," Computer Architecture 1997 ("Vajapeyam"). It is respectfully submitted that claims 1 to 28 are not anticipated by Vajapeyam for at least the following reasons.

Claim 1 relates to a method for renaming a source for use with a processor, which includes providing at least one instruction, building instruction dependency information based on the at least one instruction, caching the at least one instruction with the **instruction dependency information** to provide cached instruction information, renaming a register based on the cached instruction information to provide a renamed register, and multiplexing the instruction dependency information and the renamed register to rename the source. In this regard, the present application provides, for example, the following:

> [T]he **dependency information may be cached** to eliminate the use of the prioritized content-addressable-memories (CAMs) with the renamer arrangement and/or method of Figure 2. Caching the dependency chain information is believed to be effective for providing sequential allocation, and may be done

> using the dependency information field arrangement 400 of Figure 4. In the field arrangement 400, the first source Src1 and the second source Src2 information are provided using three (3) bits and the destination field Dst is provided using one (1) bit, which collectively provides the cached dependency chain information for use in the fast renaming apparatus, method and system of Figures 5 and 6.
>
> In particular, in the pre-decode information for providing fast renaming, the first source Src1 bits and the second source Src2 bits **indicate upon which instruction in the rename window the particular instruction depends.** A special encoding (such as, for example, '111) may indicate or otherwise denote that the specific source Src is not produced by any previous instruction in the rename window. The destination Dst bit indicates that this instruction updates the register alias table (RAT). Using this pre-decode information, the content-addressable-memories (CAMs) may be replaced by an "adder" or concatenating arrangement as shown in Figure 5. The fast renaming algorithm depends on sequential ID allocation for the renamed instructions. In particular, the system may determine a final virtual ID by concatenating the upper bits from the renamer with the lower bits from the instruction cache. It is believed that the latter approach may be faster and/or easier to implement, but may require allocation of virtual registers in larger, predefined groups having a size that depends on a power of 2.

(Specification, page 13, line 11 to page 14, line 2) (Emphasis added). Hence, instruction dependency information indicates which other instruction a particular instruction depends upon and where that other instruction is stored, rather than the actual renaming of a register.

The Vajapeyam reference, by contrast, relates to improving superscalar instruction dispatch by partitioning an instruction window into multiple blocks, partitioning a register file into a global file and several local files, and recording **register renaming information** in a trace cache. (See Vajapeyam, page 1, columns 1 to 2). In this regard, Figure 5 of Vajapeyam shows a typical entry in the trace cache, in which information is recorded that indicates which "live-on-entry" and "live-on-exit" registers are to be renamed before their use, but does not include information that indicates upon which other instruction the particular instruction depends. (See Vajapeyam, page 5, columns 1 and 2, Figure 5 and related text). It is therefore respectfully submitted that Vajapeyam does not in anyway

disclose, or suggest, caching at least one instruction with instruction dependency information, as recited in claim 1. Accordingly, Vajapeyam fails to identically disclose all of the features of claim 1 -- as it must to support an anticipation rejection. It is therefore respectfully submitted that claim 1 is allowable for at least these reasons.

Claims 2 to 7 depend either directly or indirectly from claim 1, and are therefore allowable for at least the same reasons as claim 1.

Claims 8, 15, and 22 recite features analogous to claim 1, and are therefore allowable for essentially the same reasons as claim 1.

Claims 9 to 14 depend either directly or indirectly from claim 8, and are therefore allowable for at least the same reasons as claim 8.

Claims 16 to 21 depend either directly or indirectly from claim 15, and are therefore allowable for at least the same reasons at claim 15.

Claims 23 to 28 depend either directly or indirectly from claim 22, and are therefore allowable for at least the same reasons that claim 22 is allowable.

In sum, it is respectfully submitted that claims 1 to 28 are allowable for at least the reasons discussed above. Withdrawal of the anticipation rejections of claims 1 to 28 is therefore respectfully requested.

VI. New Claims 29 to 33

New claims 29 to 33 have been added herein. No new matter has been added. Support for claims 29, 32, and 33 is found at least on page 13, lines 11 to 22, of the Specification. Support for claims 30 and 31 is found at least on page 8, lines 3 to 10, of the Specification. Claims 29 to 33 depend either directly or indirectly from claim 1, and are therefore allowable for at least the same reasons that claim 1 is allowable.

Accordingly, claims 1 to 33 are allowable.

CONCLUSION

In view of the foregoing, it is respectfully submitted that all of the presently pending claims are allowable. It is therefore respectfully requested that the objections and rejections be withdrawn since they have been obviated. All issues raised by the Examiner having been addressed, an early and favorable action on the merits is respectfully requested.

Respectfully submitted,

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Dated: 6/29/2004 By: _____

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